SURFv6, flight firmware

PSA

Overview

- SURFv6 status
- TURFv6 status
- Flight FW overview
- Progress and timeline

SURFv6

- 5x RevB delivered
- Dumb fixes:
  - Flyback diode backwards (again)
    - Flipped on existing 5
    - Fixed on B2
  - Debug RX/TX translate screwed up (unnecessary for flight)
    - Patched on existing 5
    - Fixed on B2
  - LED lightpipe interference
    - Do not fix, just cut mounting peg
  - No decoupling cap on swap ctrlr
    - Fixed on B2
- Clock chip was a bit finicky
  - Figured it out, just bad TI documentation/SW
- Everything else works great so far
  - *Still need to confirm analog performance*
  - (this was confirmed *before* but chip is now clocked differently)

TURFv6

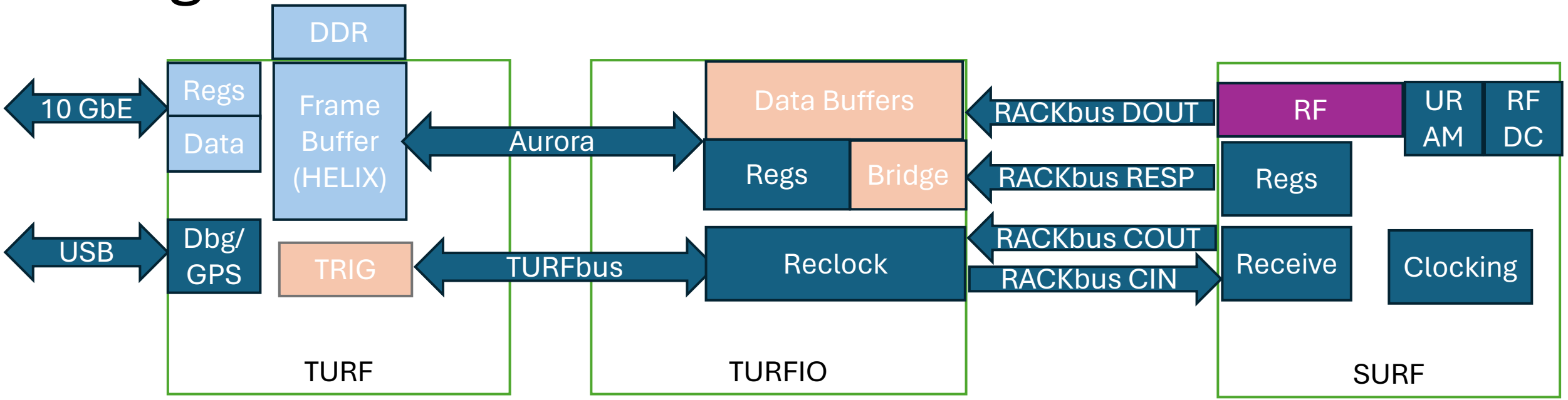
- TURFv6 works, but…
  - stupid CAD error => kills output to 2x “top” TURFIO output and 2nd 10G ethernet
  - Also idiot serial translator mistake (same one!)
- TURFv6 revB in process now
  - => 1x ready by end of June
  - => 2x ready probably Aug/Sep
- SFC<->TURF comms development in exanic_turf_test…
  - Also needs frame memory buffer integrated
  - Tested in HELIX flight successfully
- TURF<->TURFIO comms development in firmware-pueo-turf
- Needs to be merged, but shouldn’t be that hard

- **Note:** there are little bitty ‘aux boards’ inside TURF but these can be retrofit
  - **G[redacted]d[redacted]GPS (ZED-F9T)**

Flight firmware vs design test firmware

- Flight firmware has SFC commanding/data path readout/etc.
  - **Can’t copy these things on dev boards**
- Dev boards have easy high-speed data capture using PS
  - **Can’t use this on flight FW b/c of high resource usage**
- 2 types of firmware:
  - *Flight firmware:*
    - firmware-**pueo**-turfio/turf/surf6
  - *Design test firmware:*
    - firmware-zcu111/htg-zrf-hh/teb0835/rfsoc4x2/surfstandalone

Flight firmware: THE BIG OVERVIEW



RF in progress right now, some testing in design test firmware

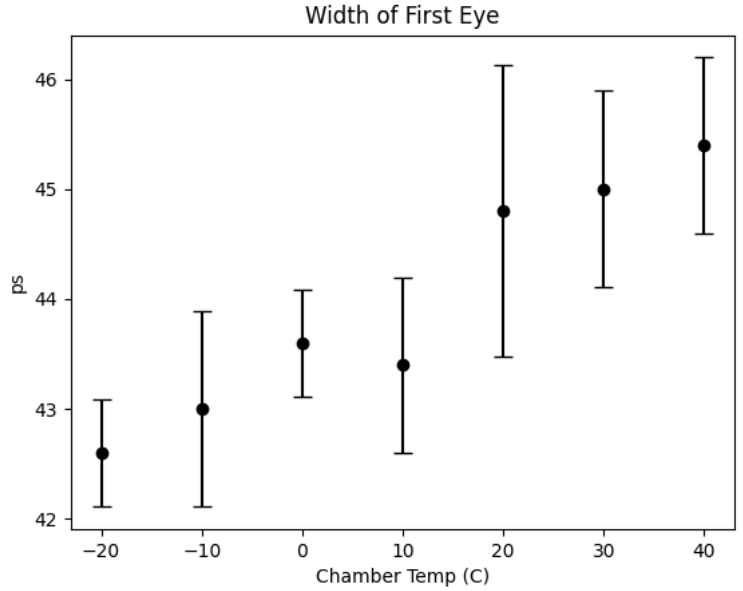
Beams need to be identified! No resource sharing right now.
RF testing covered by Lucas

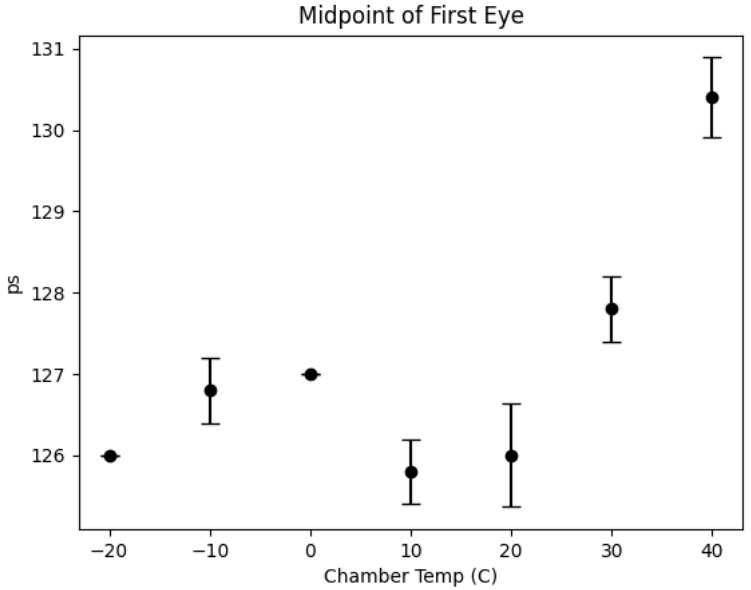
What works and is integrated?

- TURF<->TURFIO clock transfer and register comms (via debug at TURF: register access through ethernet needs to be integrated)
- TURFIO<->SURF clock transfer and register comms (via debug at SURF)
  - TURFIO bridge (to complete the TURF<->TURFIO<->SURF) in progress
- SURF RF digital portions have been tested in design test firmware (see Lucas's talk)
- All in github repos (https://github.com/barawn/)
  - firmware-pueo-surf6
  - firmware-pueo-turf
  - firmware-pueo-turfio
  - pueo-python (for control logic)

Clock transfer testing

- Will have more detail in firmware workshop
- Clock transfer is hard!
  - We have clocking restrictions due to resources in FPGA (sigh) + various frequency requirements
  - 125M -> 7.8125M -> 500M/375M/125M/7.8125M…
- SURFv6B clock transfer fully tested: alignment over temp confirmed
  - Just going to be firmware/device constants, “scan once and store”
  - e.g. combine device DNA + firmware version = calibration constants
  - Using *minimum* width over all temps, midpoint moves ~12% of width of eye over 60 deg C => no need for midpoint tracking
- Data eye is so ridiculously open not even worth considering
  - Eye is ~80% open (2.1 ns/2.7 ns), basically doesn’t shift at all with temp
- Board-to-board sync testing in progress





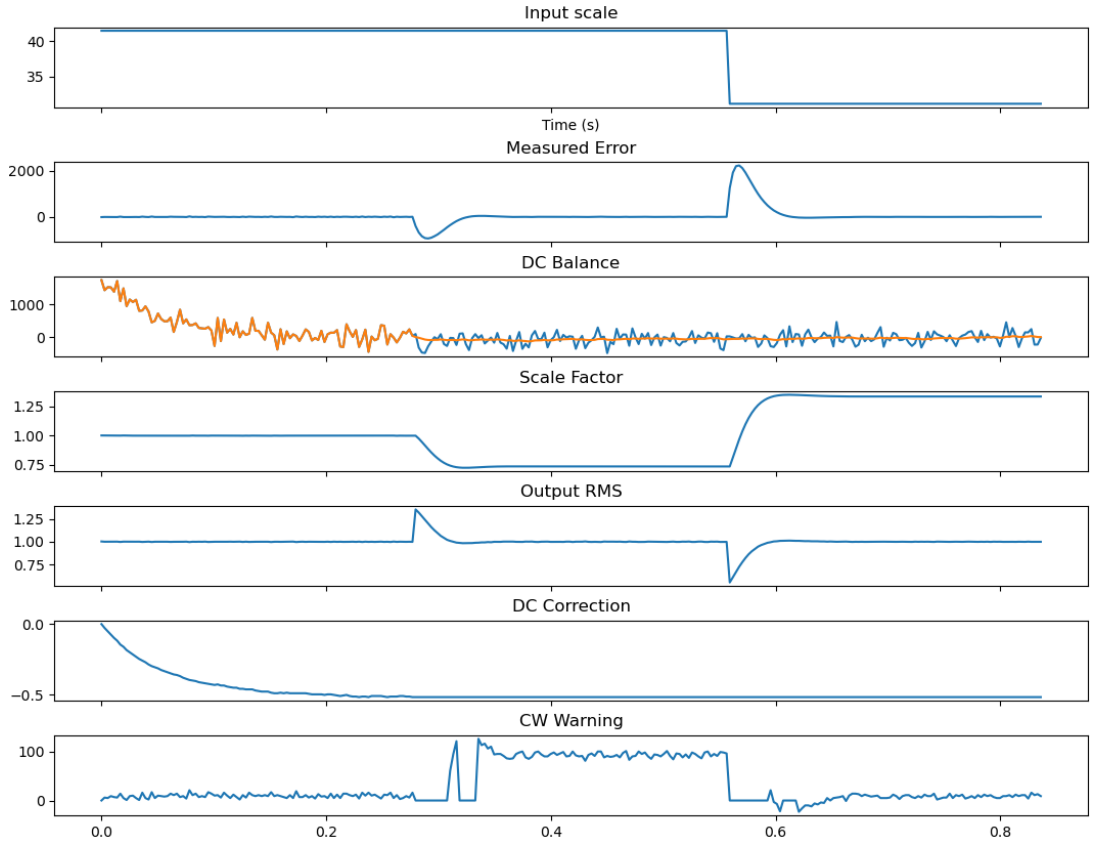
RF core testing

- Most of RF core testing being done *outside* of flight firmware
  - These are *digital* cores: they can be tested independent
  - Easier to test without the remaining PUEO framework
    - E.g. Ethernet, RF capture, Ipython notebook, etc.
  - Pure math can be tested in simulation
- Portions
  - Halfband filter ✓
  - Biquad FIR ✓ Biquad IIR □
  - AGC □
  - Beamform/square (sim) ✓
  - Thresholding □
- Biquad IIR/AGC are *tough* because need human testing: possible inputs are infinite
  - Research w/AGC core led to efficient CW pollution detection (neat)

AGC core (“12-to-5”)

- Automatic gain control takes a *variable input scale* and scales it to a *fixed* output scale
  - Output scale is in *symmetric representation* (equal pos/neg)
    - Represent *bin mindpoints* rather than *thresholds*
  - Nominal output RMS=1
  - Nominal output DC: 0
- Measures input scale 2 ways
  - Scattered RMS via custom square accumulator (random grab a sample and accumulate square via math magic)
  - Measure 2-sigma tail fractions
    - 2-sigma tail fractions used for DC corr
    - Convert tail fractions to sigma => Wichura probit approximation (-sqrt(-2logx))
- Probit/RMS difference gives a “CW warning” measure
- *Measurement* cores exist for FPGA
  - First test with loop control open and soft control
  - Hard close it later

Logic test showing normal operation, added SNR=1 CW, and finally removal of CW and scale shift



Timelines

- Biquad IIR/AGC testing in progress now => end June?
- In parallel finish SURF/TURFIO data buffer handling + basic trigger issuing by end June => “first light” of data arriving at TURF
- July => integrate TURF simulator w/real TURF so ‘basic’ data acq (no RF trigger yet) possible by 8/1

- RF trigger testing/beamforming need more work/ideas from people!
  - **Beam delays would be nice?**
  - **CW mitigation?**
  - **Approximate ANITA flight w/AGC?**
- All of this stuff is digital so it’s just toy models, not firmware